IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

APPLICANTS:	James D. Kelly *et al.*
APPLICATION NO.:	REISSUE OF USPN 5,996,036
FILING DATE:	HEREWITH
TITLE:	BUS TRANSACTION REORDERING IN A COMPUTER SYSTEM HAVING UNORDERED SLAVES
EXAMINER:	UNASSIGNED
GROUP ART UNIT:	UNASSIGNED
ATTY. DKT. NO.:	18602-06222

BOX REISSUE
U.S. PATENT & TRADEMARK OFFICE
P. O. BOX 2327
ARLINGTON, VA 22202

EXPRESS MAIL NO. EL599912565US

PRELIMINARY AMENDMENT AND STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES UNDER 37 CFR § 1.173(c)

Sir:

Prior to examination of the subject reissue patent application, please amend the patent as indicated below:

IN THE SPECIFICATION

Insert at column 1, line 4, the following sentence:

This application is a continuation-in-part of U.S. Patent Application No. 08/432,622, filed May 2, 1995, now abandoned.

IN THE CLAIMS

Add claims 18-19, as indicated below:

18. A method of avoiding deadlock in a computer system having a split-transaction bus and a single-envelope bus bridged by a bus bridge, the split-transaction bus and the single-envelope bus each having at least one master device and one slave device connected thereto, comprising:

storing data from one or more accepted bus transactions;

determining, prior to a request for a bus transaction from a requestor, if execution of such bus transaction would cause deadlock based on the stored data; and

responsive to the determination that execution of the bus transaction would cause deadlock, sending a retry signal to the bus transaction requestor.

19. An apparatus for avoiding deadlock in a computer system having a split-transaction bus and a single-envelope bus bridged by a bus bridge, the split-transaction bus and the single-envelope bus each having at least one master device and one slave device connected thereto, comprising:

a memory for storing data from one or more accepted bus transactions; and

deadlock avoidance logic coupled to the memory for determining, prior to a request for a bus transaction from a requester, if execution of the bus transaction would cause deadlock based on the stored data, the deadlock avoidance logic adapted to send a retry signal to the bus transaction requester if execution of the bus transaction would cause deadlock.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Original claims 1-17 are in the patent as issued and new claims 18-19 are pending. Support for new claims 18-19 can be found in the specification of the issued patent at cols. 9-11 *et seq*. and cols.18-19 *et seq*.

Applicant is claiming priority under 35 U.S.C. 120, from U.S. Patent Application No. 08/432,622, filed May 2, 1995, now abandoned. Applicant is also adding Michael L. Regal as an inventor under 37 C.F.R. 1.175.

Respectfully submitted,

JAMES D. KELLY

Dated: November 30, 2001

By: _____

Kirk A. Gottlieb, Reg. No. 42,596
Attorney for Applicants
Fenwick & West LLP
Two Palo Alto Square
Palo Alto, CA 94306
Tel.: (415) 875-2414
Fax: (415) 281-1350